IN THE CLAIMS

Please amend the claims 1, 6, and 21 as follows:

, L

1. (Currently Amended) In a data processing system including a plurality of processors each directly coupled via a system memory bus wherein a first processor of said plurality of processors contains a level one cache memory directly coupled to a level two cache memory which is coupled to a level three cache memory via a level three cache controller, said level two cache memory containing cache storage and tag storage and containing a circuit for SNOOPing said system memory bus, the improvement comprising:

A system memory bus interface providing a unit first dedicated path interface between said system memory bus and said cache storage and a second dedicated path interface between said system memory bus and said tag storage to a separate and dedicated port of said tag storage.

2. (Previously Presented) A data processing system according to claim 1 further comprising control logic directly coupled to said cache storage and said tag storage which provides the highest priority for said SNOOPing.

3. (Previously Presented) A data processing system according to claim 2 wherein said level two cache memory further comprises:

A duplicate tag memory.

4. (Previously Presented) A data processing system according to claim 3 wherein said plurality of processors further comprises

A plurality of instruction processors.

5. (Previously Presented) A data processing system according to claim 4 wherein said level three memory further comprises:

A level three cache memory.

- 6. (Currently Amended) A data processing system comprising:
- a. A plurality of processors including a first processor containing a level one cache memory;
- b. A level two cache memory containing a data memory and a tag memory wherein said tag memory has a first port and a second port directly coupled to said level one cache memory;
- c. A system memory bus directly coupled to said plurality of processors and directly coupled via a system memory bus

interface to said data memory and directly and independently coupled via said system memory bus interface to said tag memory via a separate and said second port of said tag memory; and

- d. A SNOOP request placed on said system memory bus and directly coupled to said tag memory.
- 7. (Previously Presented) A data processing system according to claim 6 further comprising:

A data request transferred from said level one cache memory to said level two cache memory.

8. (Previously Presented) A data processing system according to claim 7 further comprising:

Control logic within said level two cache memory which provides priority of said SNOOP request over said data request.

- 9. (Previously Presented) A data processing system according to claim 8 further comprising:
- a. A level one tag memory located within said level one cache memory; and
- b. A duplicate tag memory within said level two cache memory which maintains a duplicate of information within said level one tag memory.

- 10. (Previously Presented) A data processing system according to claim 9 wherein said SNOOP request is directly coupled to said duplicate tag memory.
- validity of data within a level one cache memory of a processor having a level one tag memory directly coupled to a level two cache memory containing a tag memory and a data memory wherein said level two cache memory is directly coupled via a system memory bus interface to a system memory bus to said data memory via a first dedicated path and to said tag memory via a second dedicated path within said system memory bus interface comprising:
 - a. Formulating a SNOOP request;
- b. Presenting said SNOOP request on said system memory bus
 to said level two cache memory;
- c. Routing said SNOOP request directly to said tag memory via said second dedicated path; and
 - d. Processing said SNOOP request.
- 12. (Original) A method according to claim 11 further comprising:
- a. Presenting a data request from said level one cache memory to said level two cache memory; and

- b. Granting priority to said SNOOP request over said data request.
- 13. (Previously Presented) A method according to claim 12 further comprising:

Maintaining a duplicate copy of said level one tag memory within a duplicate tag memory within said level two cache memory.

14. (Previously Presented) A method according to claim 13 further comprising:

Routing said SNOOP request to said duplicate tag memory.

15. (Previously Presented) A method according to claim 14 further comprising:

Processing said SNOOP request regarding said duplicate tag memory.

- 16. (Previously Presented) An apparatus comprising:
- a. Executing means for executing program instructions;
- b. Level one caching means directly coupled to said executing means for level one caching data;
- c. Requesting means directly coupled to said executing means and said level one caching means for requesting a data element if said executing means requires requesting of said data

element and said level one caching means does not contain said data element;

- d. Level two caching means directly coupled to said requesting means for level two caching;
- e. Storing means located within said level two caching means for storing level two caching data;
- f. Maintaining means located within said level two caching means for maintaining level two tags; and
- g. SNOOPing means directly coupled via a dedicated path separate from said storing means to said maintaining means for directly SNOOPing said level two tags.
- 17. (Previously Presented) An apparatus according to claim 16 further comprising:
- a. Granting means directly coupled to said storing means and said maintaining means for granting priority to a SNOOP request over said data element request.
- 18. (Previously Presented) An apparatus according to claim 17 further comprising:
- a. Bussing means directly coupled to said level two caching means for bussing system memory data;

- b. First interfacing means directly coupled to said bussing means for interfacing said bussing means directly to said storing means; and
- c. Second interfacing means directly coupled to said bussing means for interfacing said bussing means directly to said maintaining means.
- 19. (Previously Presented) An apparatus according to claim
 18 further comprising:
- a. Recording means located within said level one caching means for recording level one tags; and
- b. Duplicating means located within said level two caching means and directly coupled to said recording means for duplicating said level one tags.
- 20. (Previously Presented) An apparatus according to claim 16 further comprising:
- a. SNOOPing means directly coupled to said bussing means and said duplicating means for SNOOPing said duplicating means.
- 21. (Currently Amended) A data processing system having a plurality of processors comprising:
 - a. a main memory;
 - b. a system bus responsively coupled to said main memory;

- c. a plurality of cache memory units wherein each of said plurality of cache memory units is dedicated to a different one of said plurality of processors;
- d. a plurality of cache data storage units wherein each of said plurality of cache data storage units is located in a different one of said plurality of cache memory units;
- e. a plurality of tag storage units wherein each of said plurality of tag storage units is located in a different one of said plurality of cache memory units and each of said tag storage units has a plurality of ports including one of said plurality of ports dedicated to snooping;
- f. a plurality of first direct paths wherein each of said plurality of first direct paths directly couples a different one of said plurality of cache data storage units to said system bus via within a system bus interface; and
- g. a plurality of second direct paths wherein each of said plurality of second direct paths directly couples a different one of said plurality of tag storage units via said one of said plurality of ports dedicated to snooping to said system bus via within said system bus interface.
- 22. (Original) A data processing system according to claim 21 wherein at least one of said plurality of processors further comprises an instruction processor.

- 23. (Original) A data processing system according to claim 22 wherein said at least one of said plurality of processors further comprises a dedicated level one cache memory.
- 24. (Original) A data processing system according to claim 23 wherein said dedicated level one cache memory further comprises a read only instruction cache memory.
- 25. (Original) A data processing system according to claim 24 wherein said dedicated level one cache memory further comprises a read/write operand cache memory.